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PCB Topics and Tips for Better EMI and SI Performance

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Electronic & Software Design, Inc.

- John R. Severson, PE
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- 35+ years designing electronic circuits, systems PC boards, RF, Design for EMC, and software
- Broad experience in many markets
  - Military Electronics
  - Analog/Digital Instrumentation, Metrology
  - Medical Image processing and graphics
  - CCTV, Analog and digital audio, video and security
  - Adaptive technology for persons with disabilities
  - Agricultural IoT, specialty RFID, and RF modules

Electronic & Software Design, Inc.

- John Severson, PE – 30 years designing electronic systems and PC boards
- PCBs with high speed logic, precision mixed signal, wireless, video, CCD/digital imaging, graphics, LCD display monitor controllers
- Embedded Microcontrollers and Linux Software
- Design for EMC, RF Modules integration, RFID systems
- SolidWorks (3D) and Altium Designer

PCB Topics and Tips for Better EMI and SI Performance

- The focus of this presentation is on some key issues to **improve performance** of **PCB layouts** from an **EMI**, **Signal (and power) Integrity** perspective.
- There are **many commonalities**, and often **following the tips for EMI** can **improve SI** and **vice-versa**.
- **PI** is a win for **both**, and for board **performance** and **reliability** in general
- Some **Practical Tips**

EMI / EMC Issues

- **EMI** requires both a noise **source** and an **antenna**.
- **Digital signals** and **switching power** supplies have **high harmonic content**.
- **EMI** problems are most often from **common mode noise**
- **Crosstalk** – noise from a source can **couple** onto a **potential antenna**
- **Ground or Power Bounce** lead to common mode noise
- For **EMI**, **uA** and **uV** can be problematic. **Immunity** can encounter **A** and **kV** levels.

SI – Signal Integrity Issues

- **Distortion** – Attenuation, Noise, Timing distortion, Bandwidth limiting -- Parasitics
- **Reflections** (impedance discontinuities)
- **Crosstalk** between signals affects **data** and **timing**
- **Ground** or **Power Bounce** distort signals and timing
- Power supply **distribution issues** or **collapse**
- **Interference** (Self and System EMC)

Some EMI and SIPI Issues in Common

- The **Hidden Schematic** – real parts have parasitics
- **Fast Rise Times** and **High Clock Speeds** magnify the issues
- **Impedance discontinuities** (and failure to control the **return path**) reduce SI and increase EMI
- Poor and **Inadequate Power Bypassing reduce SI** and **increase EMI**
- **Balancing** (differential) **improves** both **SI** and **EMI**

Some EMI and SI Divergent Issues

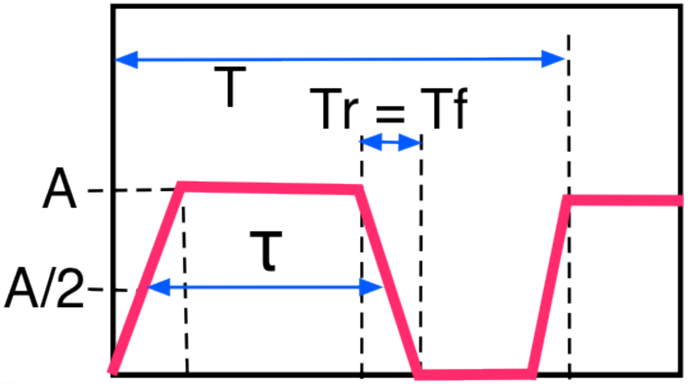
- EMI **Filters limit bandwidth** to **reduce harmonics** – Can **reduce signal integrity** if **too aggressive**
- A **few mV** of noise is **unlikely to cause SI issues**, but a **few uV** of noise can **cause an EMI failure**.
- **Faster Rise Times** are **needed** for **high data rates** but also significantly **increase problematic harmonics** for **EMI**
- (My observation is that SI is generally more easily modeled and simulated than EMI)

Frequency, Wavelength, and the Time Domain

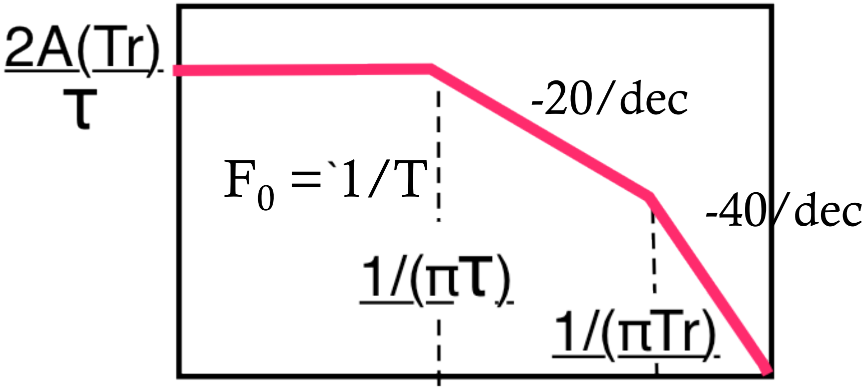
λ is less in PCB ~ $\frac{1}{\sqrt{\varepsilon_r}}$

- **λ = 300/f(MHz)** in meters (in air)
- Consider the design at **DC** – **1MHz** – **100MHz – 1GHz** etc.
- The maximum spectrum from a digital signal can be estimated

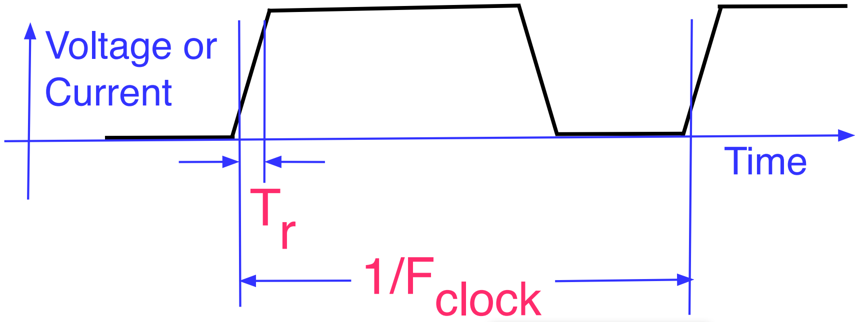
Digital Signal Time domain



Frequency domain (bounds)



Rise Time, Frequency and Scale

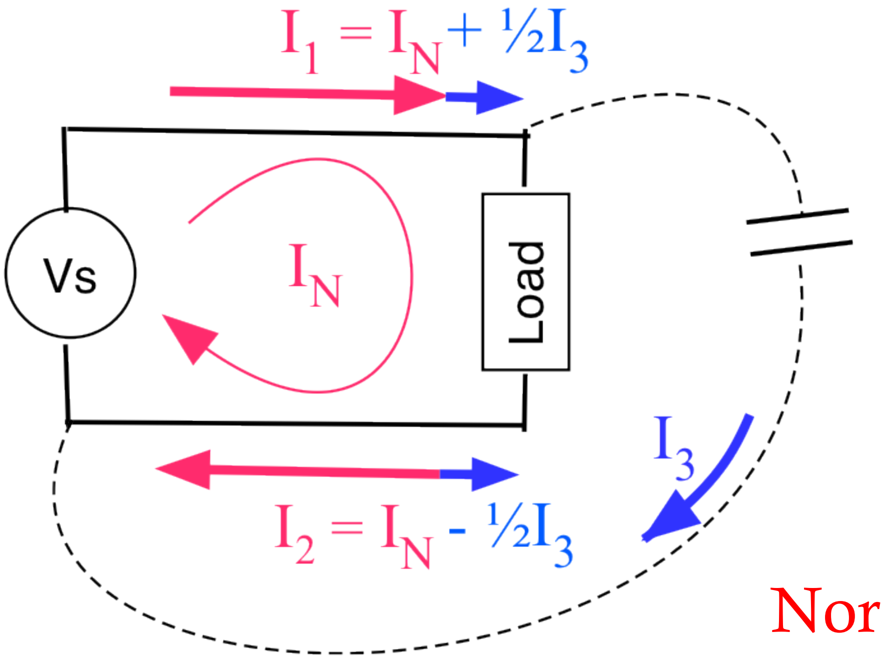


Critical Len is distance where Tprop is < 20% of Trise

λ / 20 is a conservative estimate of "electrically small"

Clock Frequency	**Rise Time (1/10)**	**Critical Len*** (in) FR4	**Wavelen λ (m)** Air	**10th Harm**	**λ /10 (m)** Air	**λ /20** (in) FR4
1 MHz	100nS	100	300 m	10 MHz	30 m	290
10 MHz	10nS	10	30 m	100 MHz	3 m	29
100 MHz	1nS	1	3 m	1 GHz	30 cm	2.9
1 GHz	100pS	0.1	30 cm	10 GHz	3 cm	0.29
10 GHz	10pS	0.01	3 cm	100 GHz	3 mm	0.029

Normal and Common Mode



An **unbalance** (e.g., stray capacitance) can introduce a **common mode current**

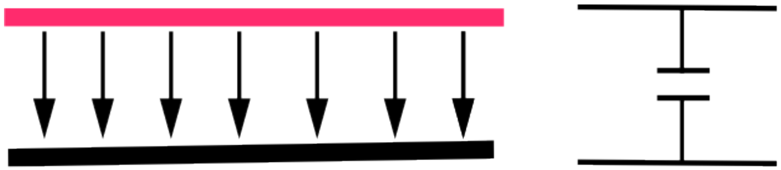
Normal Mode = I_N

Common Mode = I_{CM} = ½I_3

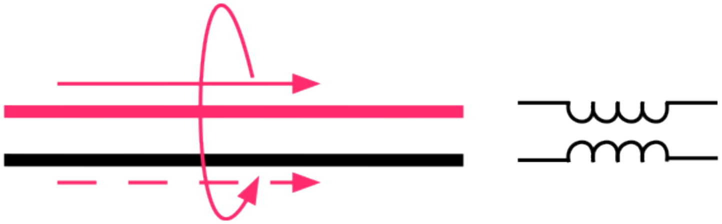
I_{CM} reduces **signal integrity** and causes **EMI**

Crosstalk and Coupling Mechanisms

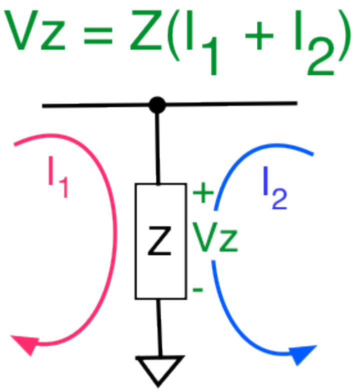
- **Capacitive** (Electric Field)



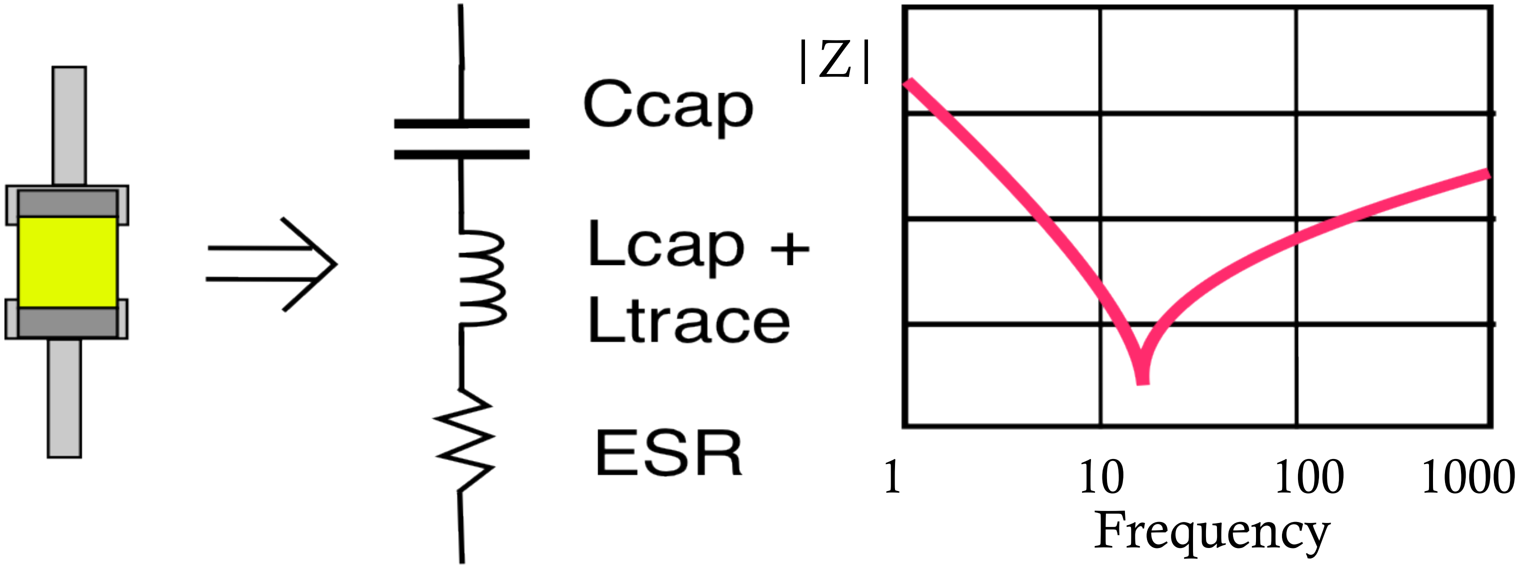
- **Inductive** (Magnetic Field)



- **Common** (Shared) **Impedance**

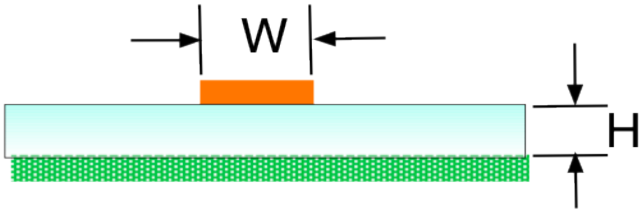


Simplified Real Component Model for SMT ceramic capacitors

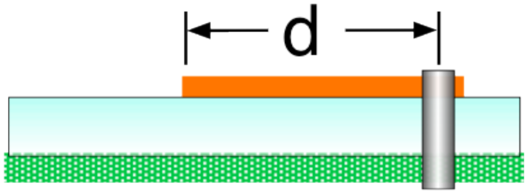


Parasitic characteristics of capacitor and trace/via. The graph shows a sample “self-resonance” where impedance rises after hitting a minimum.

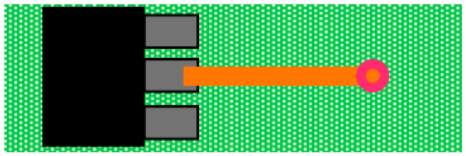
Trace and Via RF Impedance



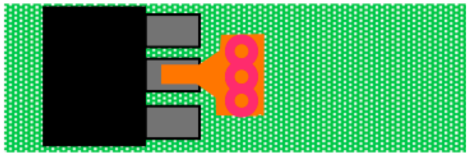
E.g, $W=20$ mils,
$H=60$mils; $L\approx16$nH/in



A typical (16 mil) via
inductance $L\approx0.9$ nH

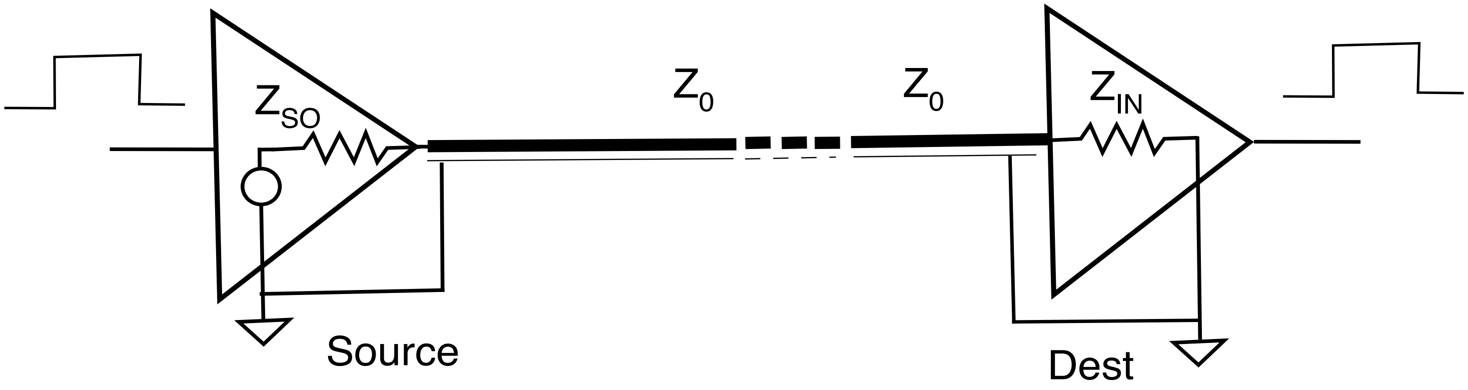


For a 3/4" trace and a
single via, $L \approx 13$ nH
1t 100 MHz, $X_L \approx 8\ \Omega$

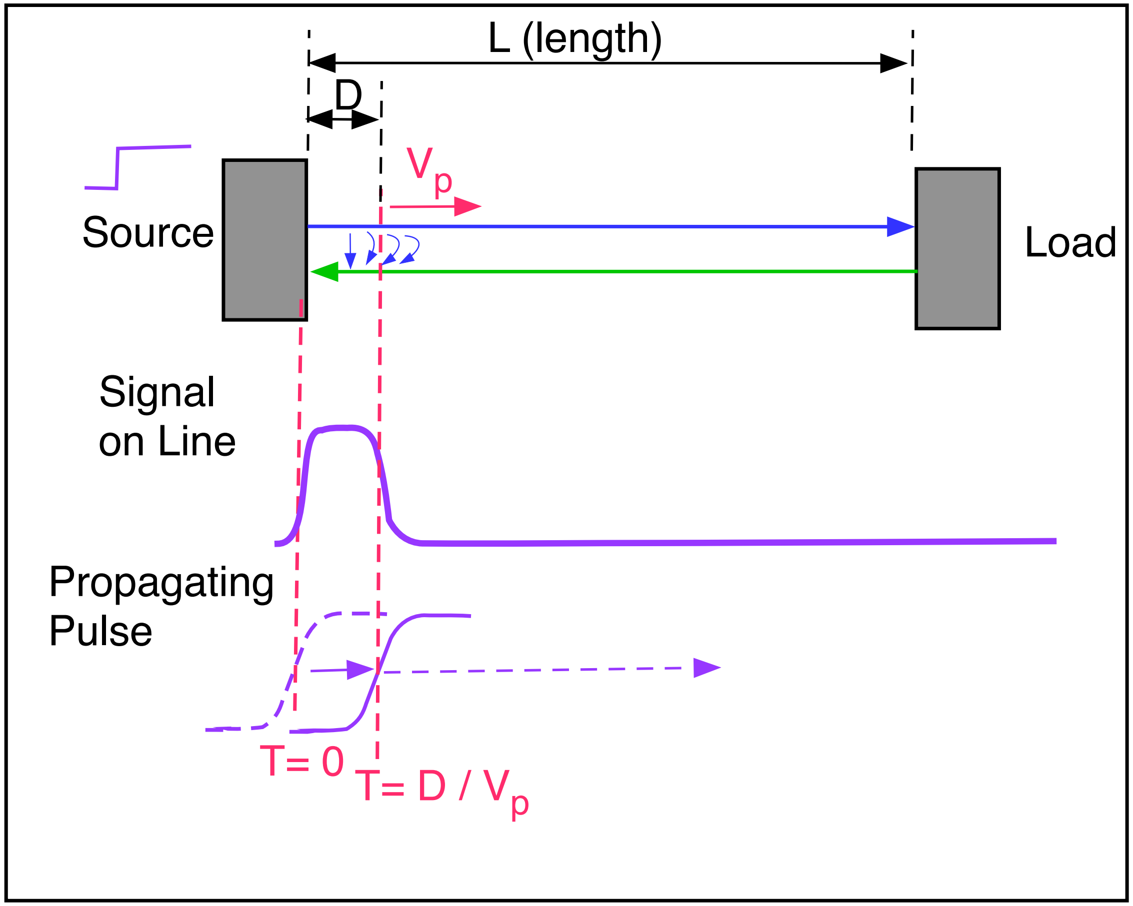


A very short, wide trace and
multiple vias could be 10X less!

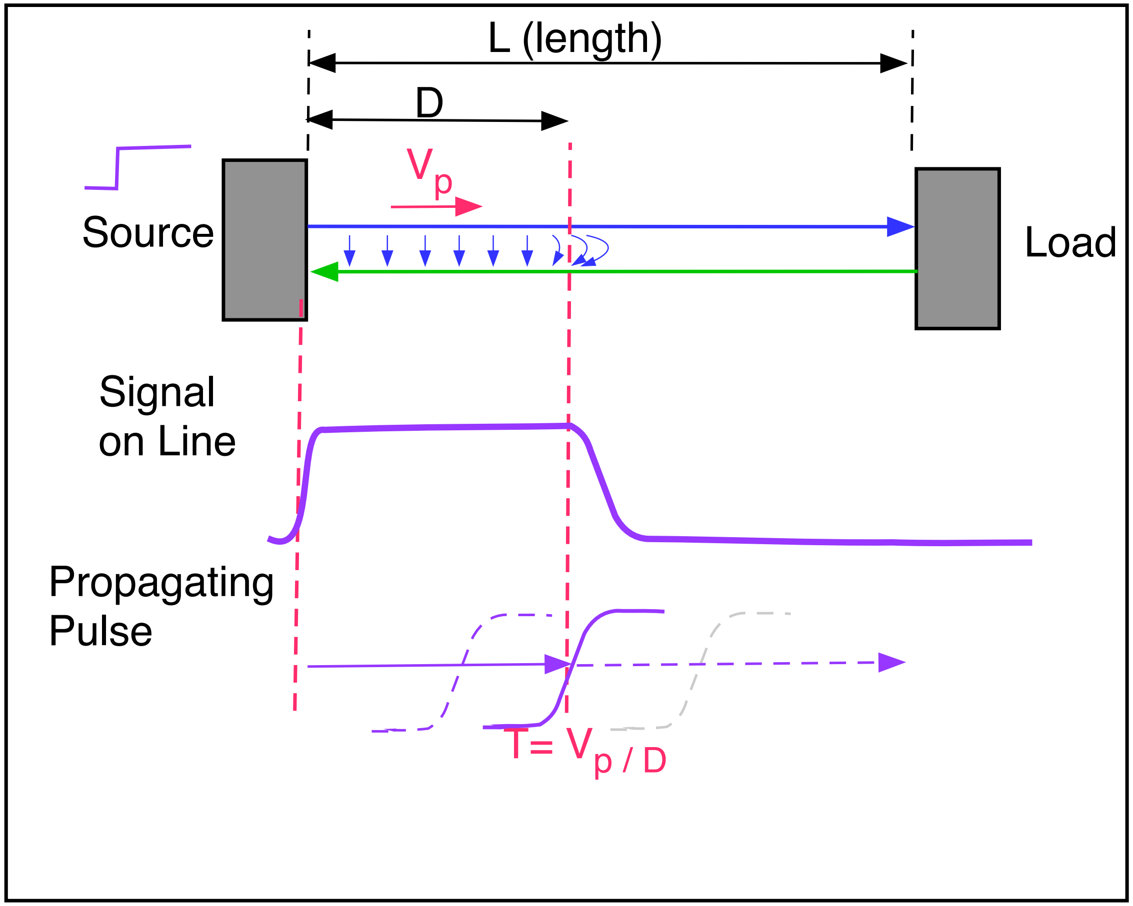
Quick Review - Transmission Lines, Terminations and Reflections



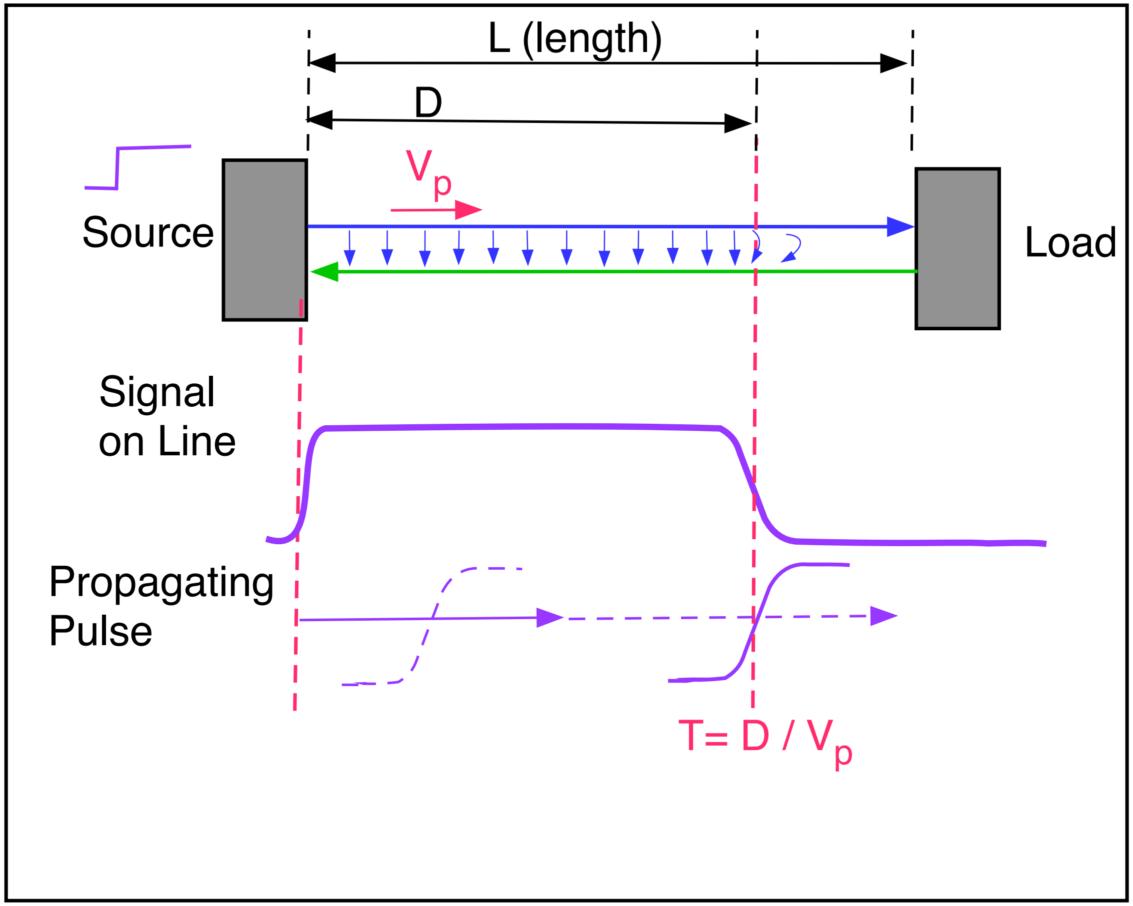
Transmission Line propagation



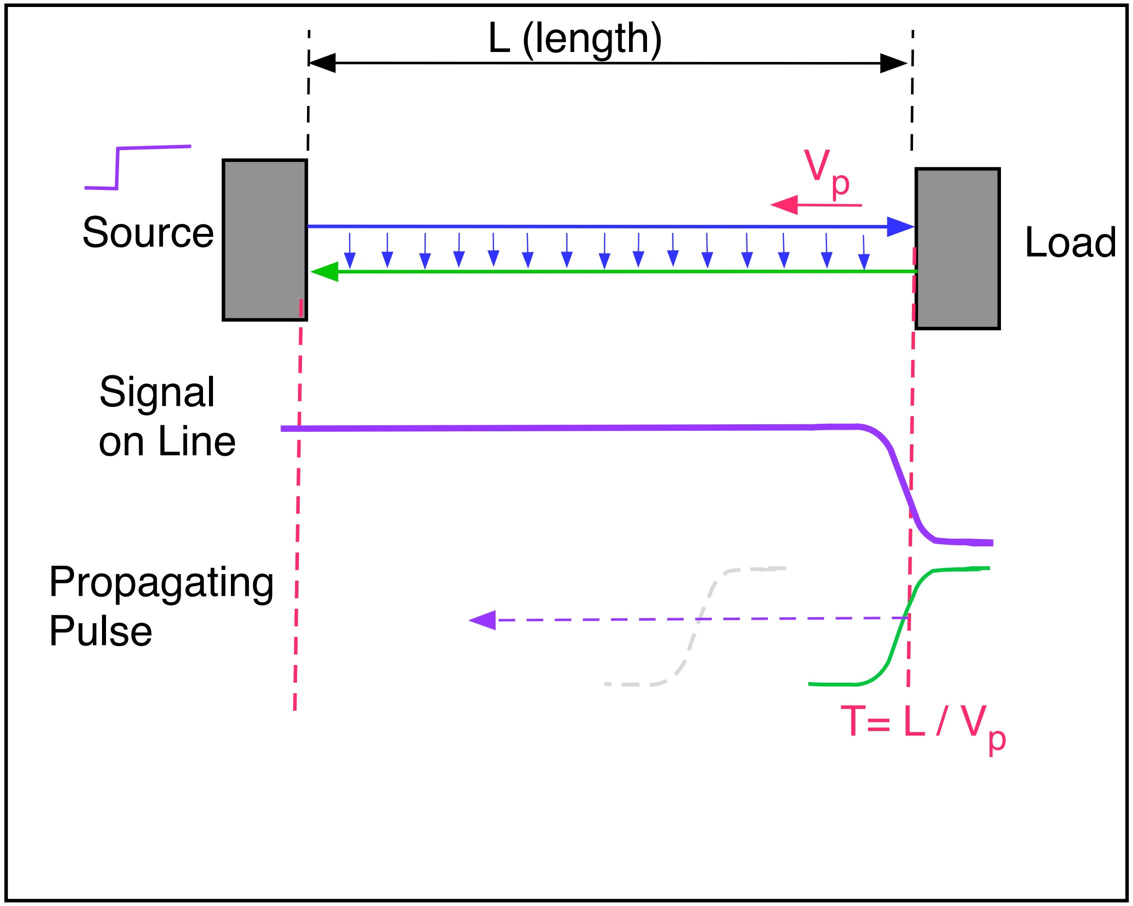
Pulse travels down the line...



Building field as it propagates…



When it arrives at the end, a reflection occurs it there is an impedance mismatch.



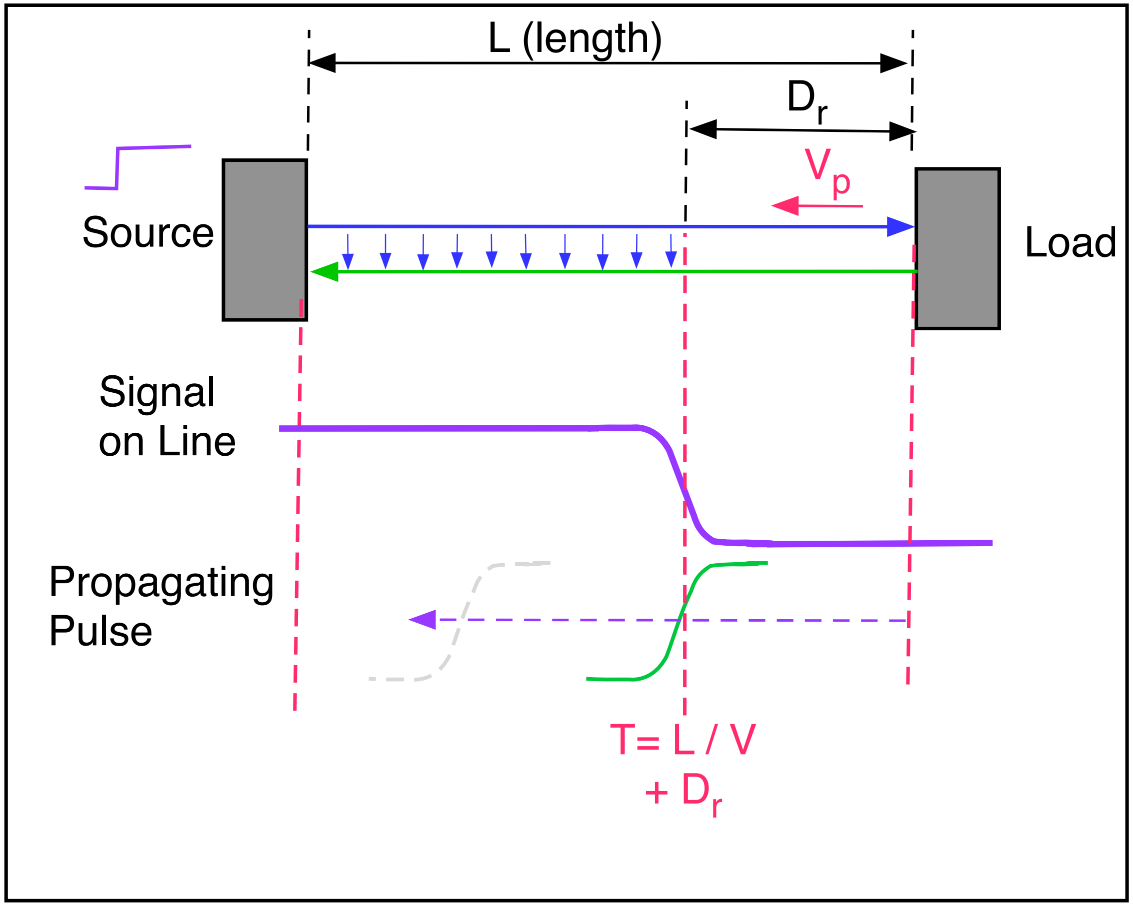
Zload = Zo
- No reflection

Zload > Zo
- Positive reflection

Zload < Zo
- Negative reflection

Reflection is
$\rho = (Z\text{-}Zo)/(Z+Zo)$

The Reflected pulse travels back toward the source, altering the field as it goes

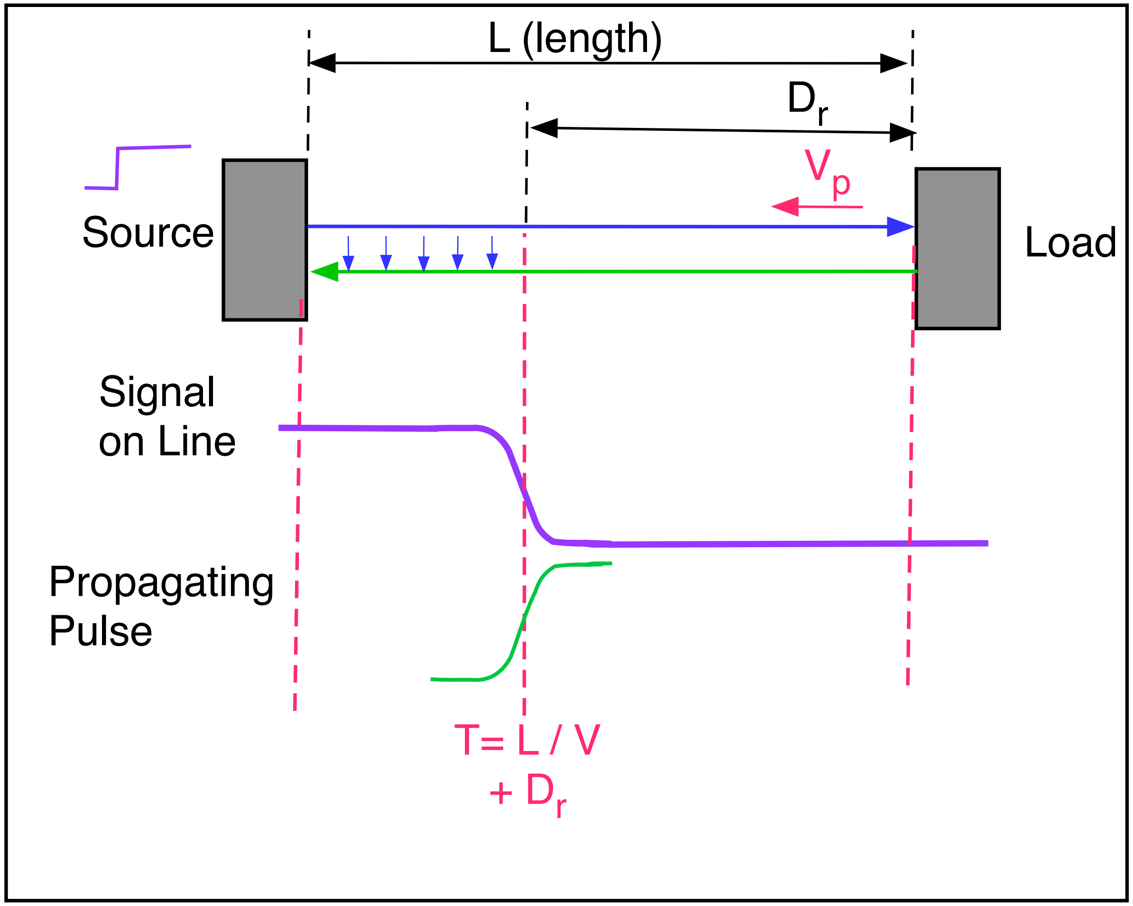


Zload < Zo

- Negative reflection

(this example pulse is for a short Z=0)

The Reflected Pulse Propagates back toward the Source…



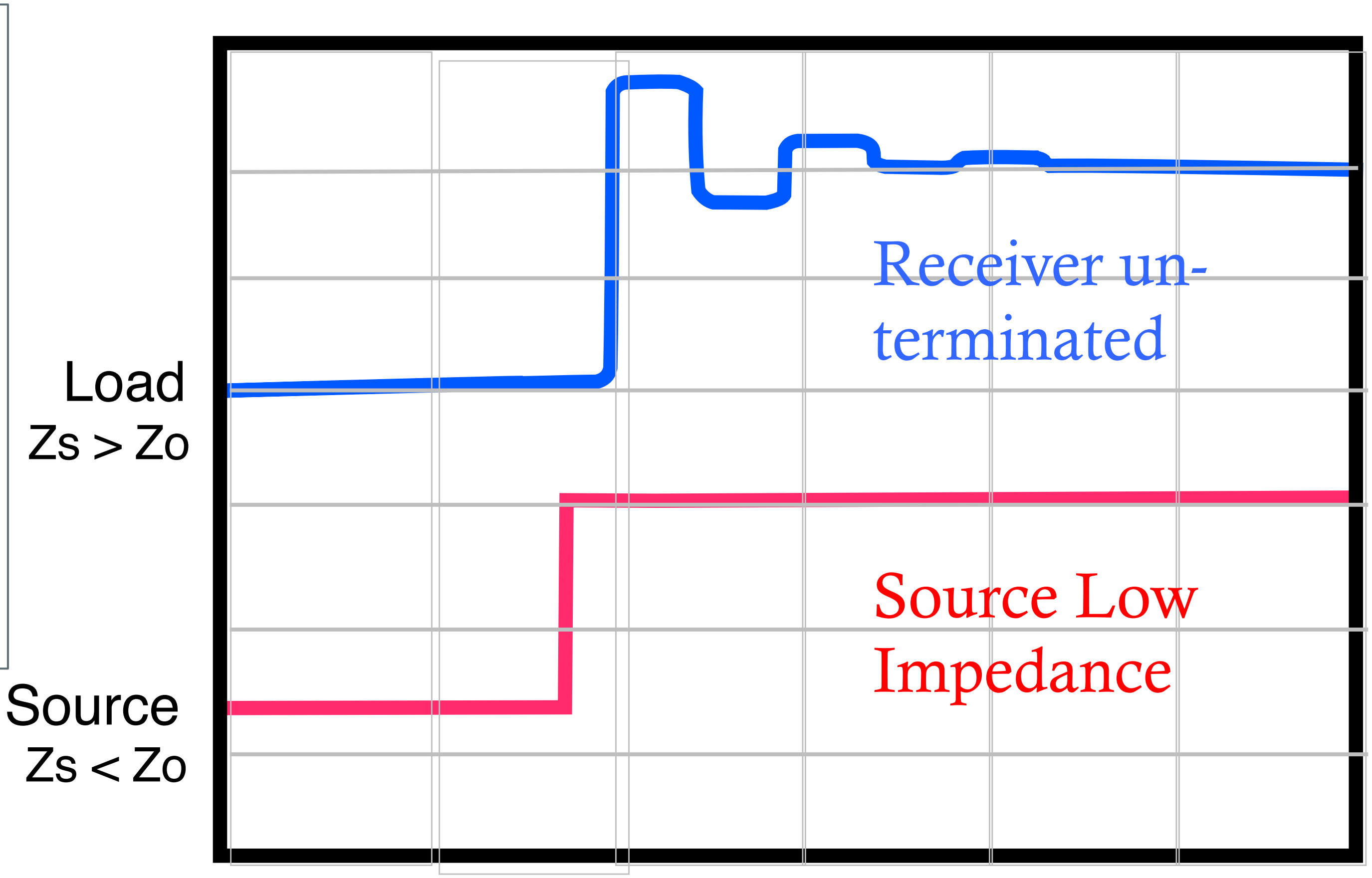
This example shows a negative going pulse since the load was low Z.

What if the source was low Z and the load High Z…

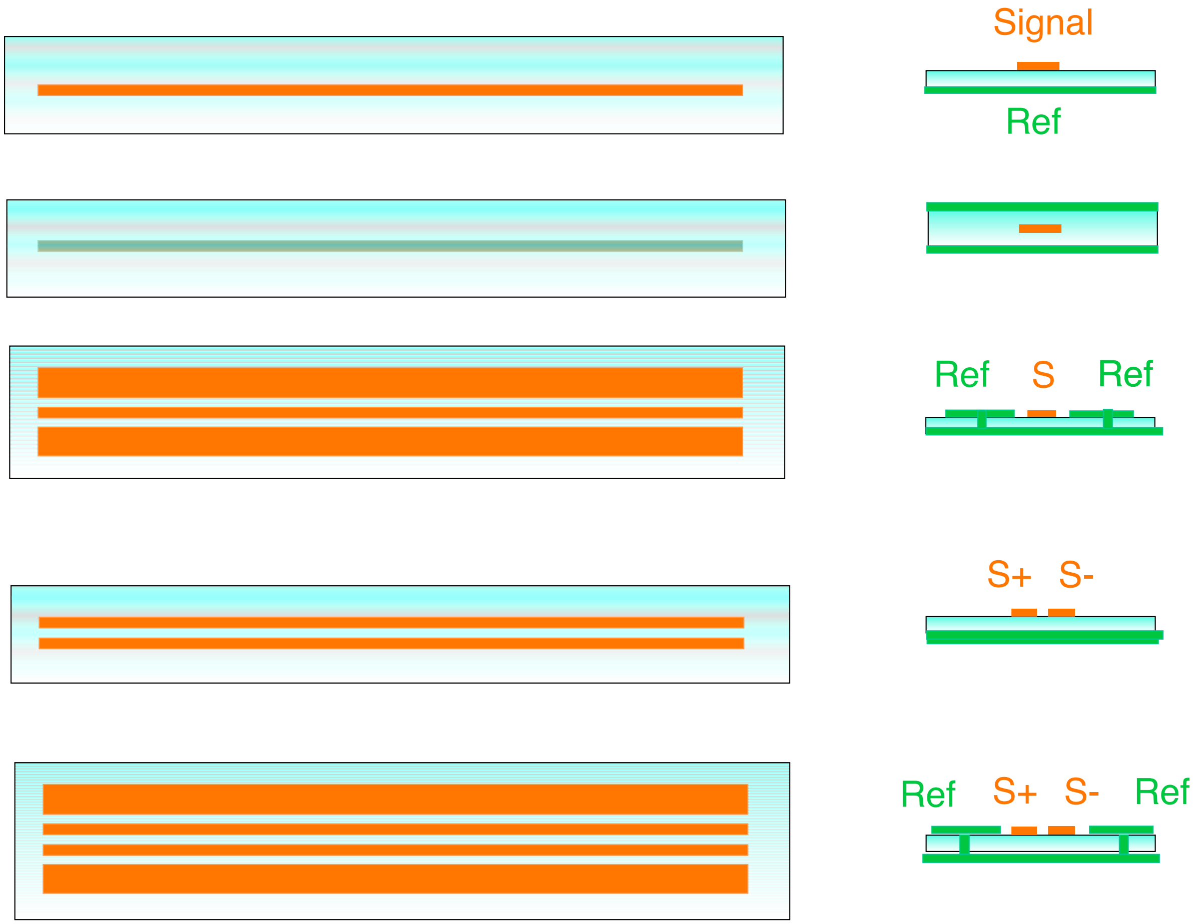
Impedance Discontinuities can look like "Ringing"

Signal reflects back and forth until reflections die out.

On a short line, looks under-damped RLC



Common Planar Transmission Lines



Microstrip

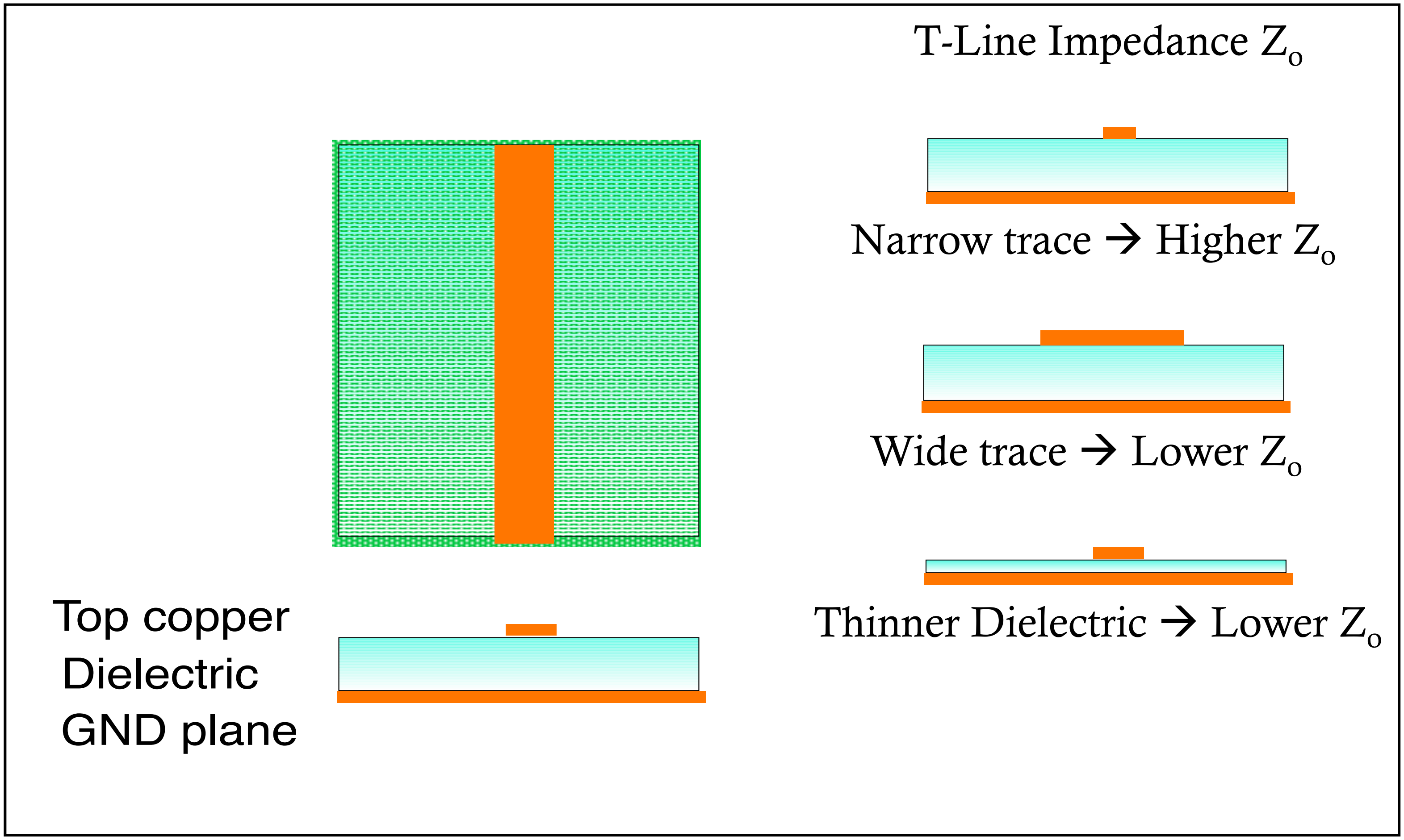
Stripline

Coplanar
Waveguide

Differential
Microstrip

Diff. Coplanar
Waveguide

Trace over GND Plane – the Microstrip T-Line



T-Line Impedance Z_o

Top copper
Dielectric
GND plane

Narrow trace → Higher Z_o

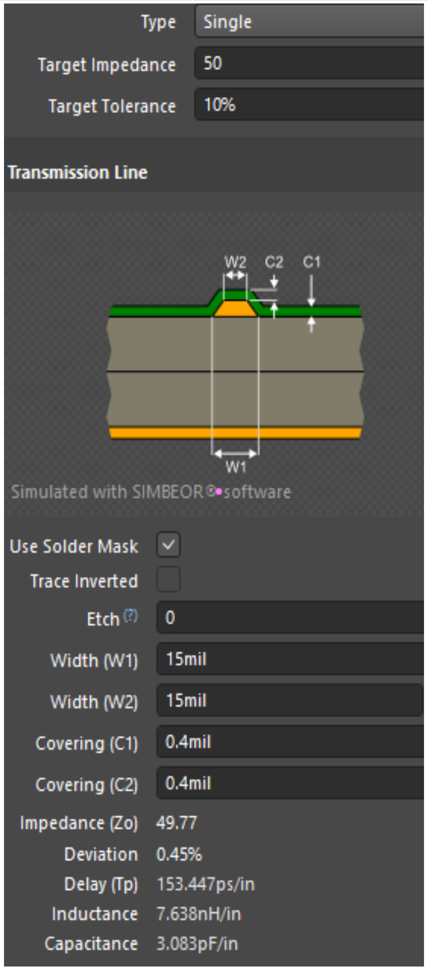
Wide trace → Lower Z_o

Thinner Dielectric → Lower Z_o

Trace Impedance

- Reasonable approximate formulas exist for **Microstrip** and **Striplines**.
- Use of **a 2D field solver** is much better and is **highly recommended** – Built into Altium *Designer.*
- There are online 2D solver options.

2D Field Solver Example

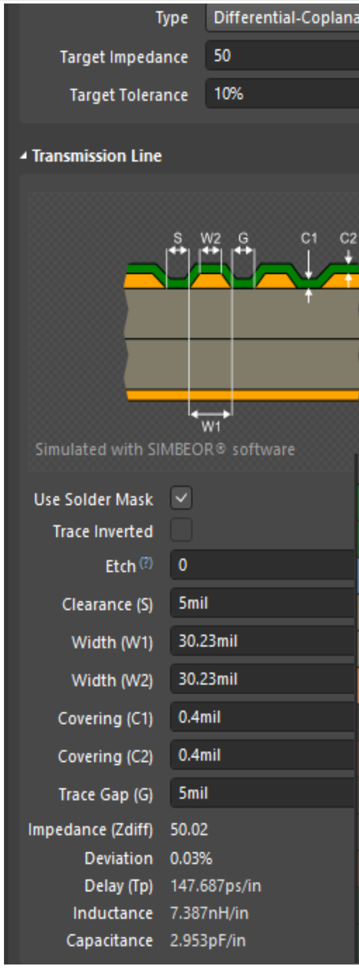


Type: Single
Target Impedance: 50
Target Tolerance: 10%

Transmission Line

Simulated with SIMBEOR® software

Use Solder Mask: ☑
Trace Inverted: ☐
Etch: 0
Width (W1): 15mil
Width (W2): 15mil
Covering (C1): 0.4mil
Covering (C2): 0.4mil
Impedance (Zo): 49.77
Deviation: 0.45%
Delay (Tp): 153.447ps/in
Inductance: 7.638nH/in
Capacitance: 3.083pF/in



Type: Differential-Coplanar
Target Impedance: 50
Target Tolerance: 10%

Transmission Line

Simulated with SIMBEOR® software

Use Solder Mask: ☑
Trace Inverted: ☐
Etch: 0
Clearance (S): 5mil
Width (W1): 30.23mil
Width (W2): 30.23mil
Covering (C1): 0.4mil
Covering (C2): 0.4mil
Trace Gap (G): 5mil
Impedance (Zdiff): 50.02
Deviation: 0.03%
Delay (Tp): 147.687ps/in
Inductance: 7.387nH/in
Capacitance: 2.953pF/in

From Altium Designer 2023 built into layer stack manager

#	Name	Material	Type	Weight	Thickness	Dk
	Top Overlay		Overlay			
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5
1	Top Layer		Signal	1oz	1.4mil	
	Dielectric 4	PP-013	Prepreg		3.8mil	4.3
	Dielectric 2	PP-016	Prepreg		4.6mil	4.4
2	Layer 1	CF-004	Plane	1oz	1.378mil	
	Dielectric 1	Core-042	Core		39mil	4.6
3	Layer 2	CF-004	Plane	1oz	1.378mil	
	Dielectric 3	PP-016	Prepreg		4.6mil	4.4
	Dielectric 5	PP-013	Prepreg		3.8mil	4.3
4	Bottom Layer		Signal	1oz	1.4mil	
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5
	Bottom Overlay		Overlay			

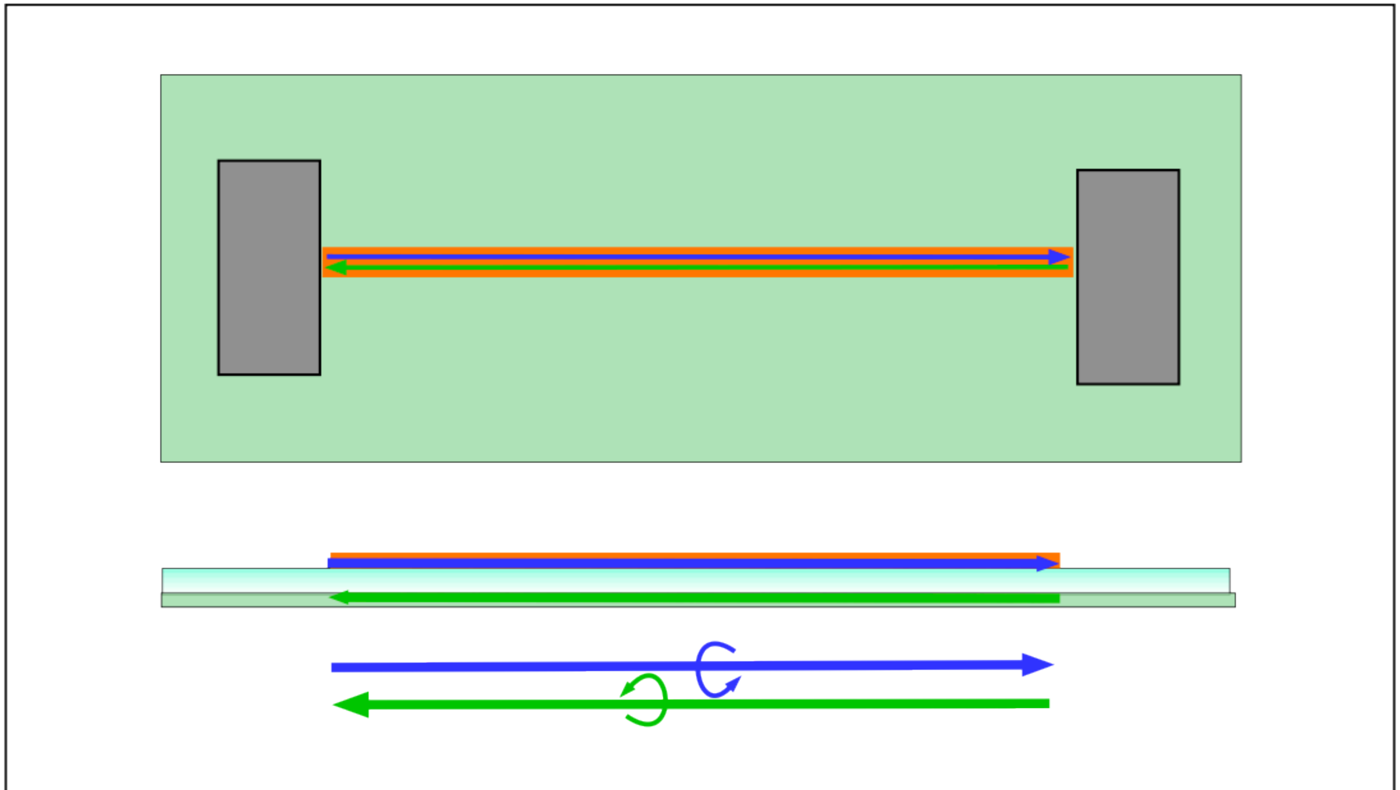
PC Board Stack-up

- Good **PCB Stack Up** is a **must do** starting point for **good EMI and SI** performance
- Think of the **stackup** as the **foundation**, like for building
- Most important is **clean reference (gnd) planes**. They are essential for **low return impedance**, **controlled impedance** traces, effective **bypassing**, **minimizing ground bounce**, and reducing **common mode noise**.
- All **high speed routes** should be over an **uninterrupted reference plane.**

Avoid Impedance Discontinuities!

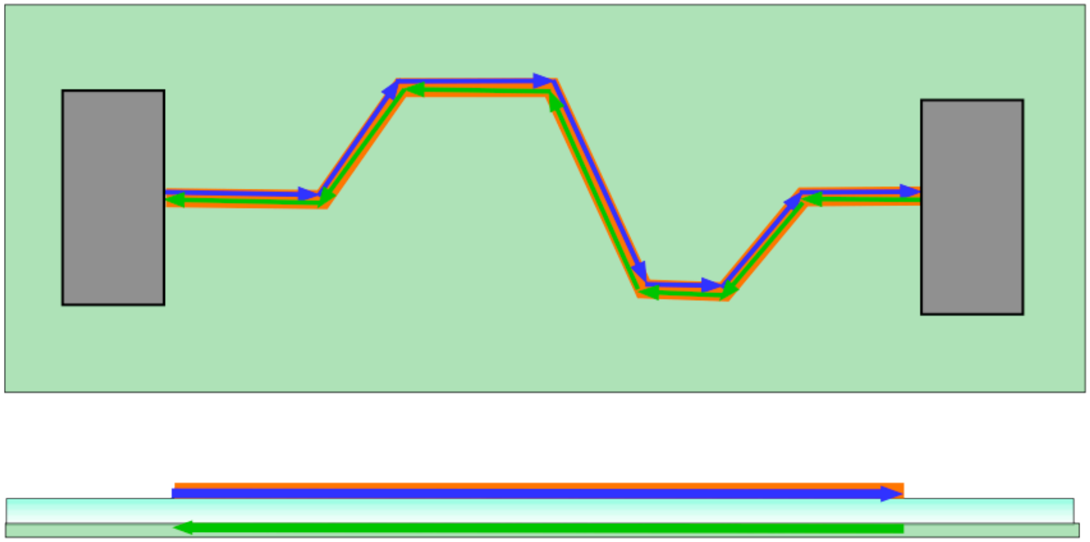
- **Routing** over a **gap** in the **plane** or a "**Swiss Cheese**" Reference Plane
- **Changing Reference Planes** (e.g., via to another layer)
- A **change** of **line width** on the same layer
- **Stubs**
- **Un-terminated** Transmission Lines

Trace over continuous ground plane – Microstrip – RF return current follows signal



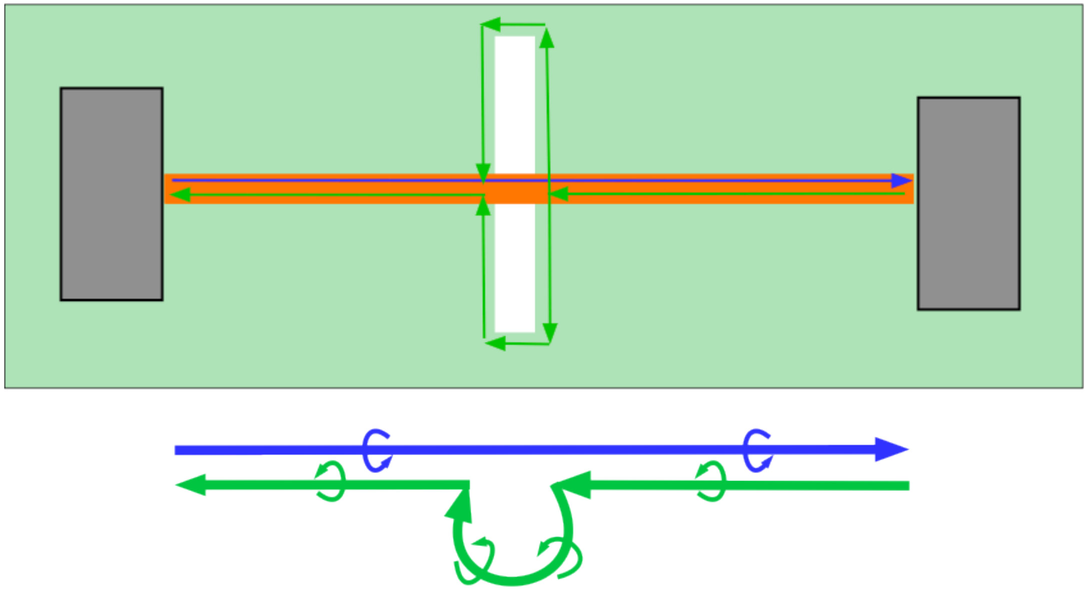
If currents are balanced, fields cancel

Trace over continuous ground plane – Microstrip – RF return current follows signal



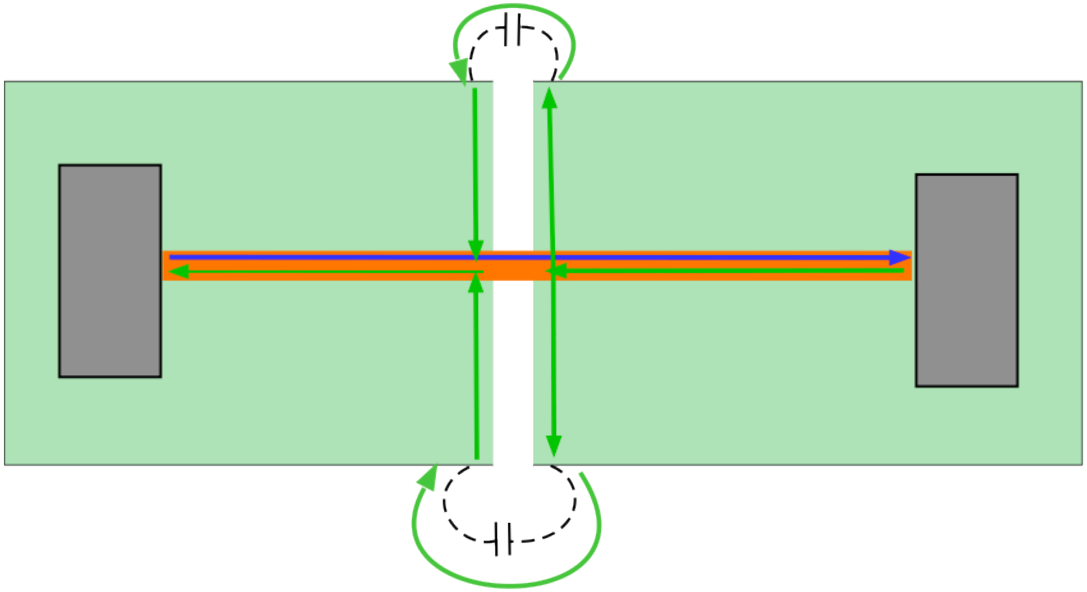
At RF Frequencies, the return current (in the ground plane) closely follows the signal path, so long as the ground plane is *continuous*.

Trace over discontinuous ground plane -- routing over gaps!



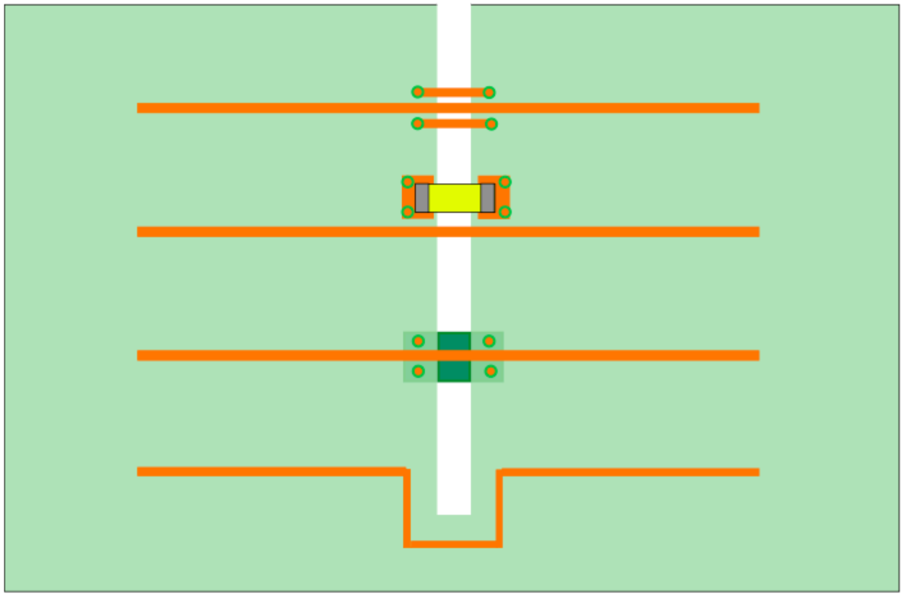
A large loop is created, currents are no longer balanced, and a common mode current is introduced in the ground plane.

…Even worse with isolated planes

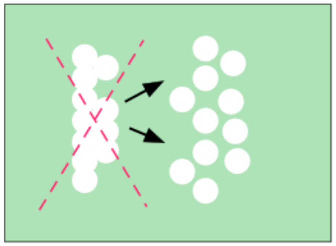


The return current **will** find a way back to the source, e.g., through stray capacitance. A significant antenna may be created.

Create a low impedance path for RF return currents

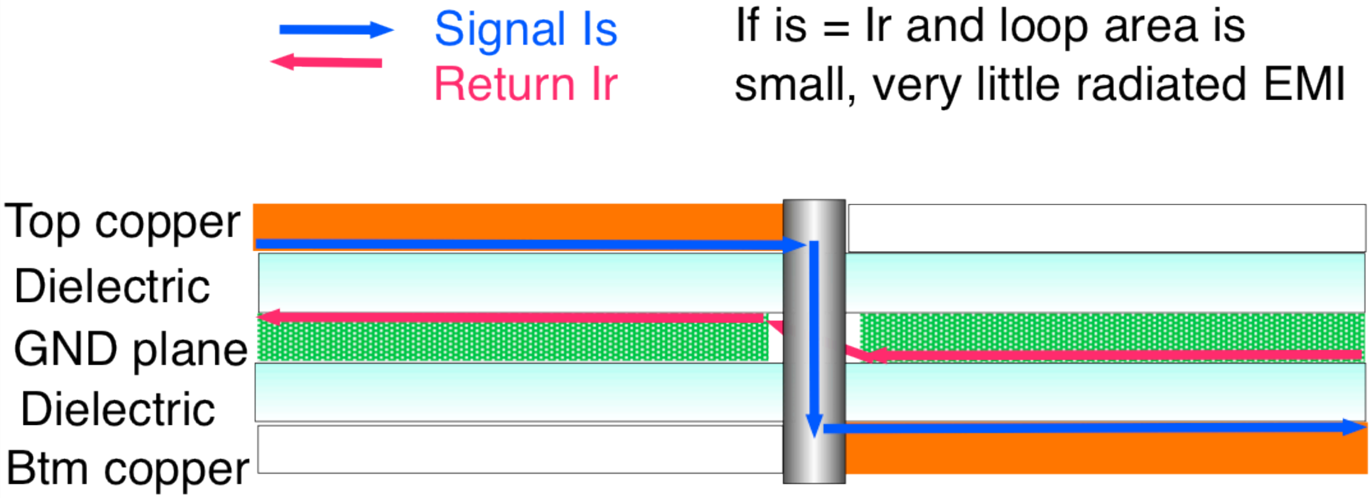


- Short "stitch" trace(s)
- RF Capacitor across gap
- Stitch to another plane
- Route around the gap **(Best)**



Watch for **unintentional gaps** in planes! ("**Swiss Cheese**" Plane)

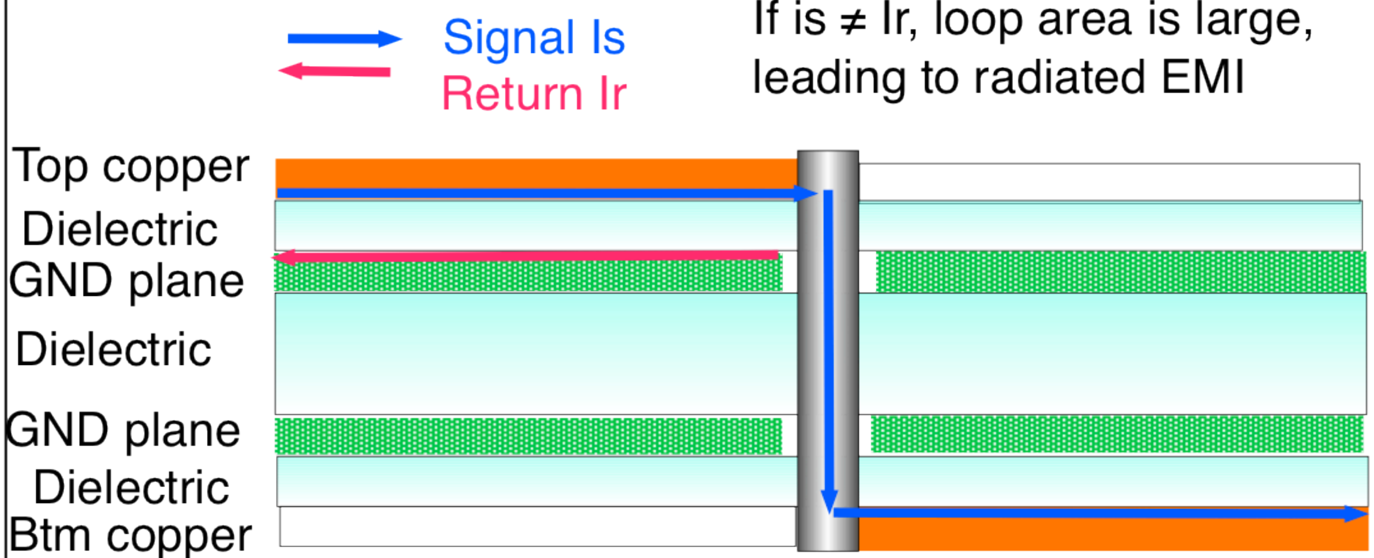
Changing Reference Planes



If is = Ir and loop area is small, very little radiated EMI

Case 1: Signal is via'd from one side of a reference plane to the other side of the
-- OK as the return path is continuous and can closely follow signal

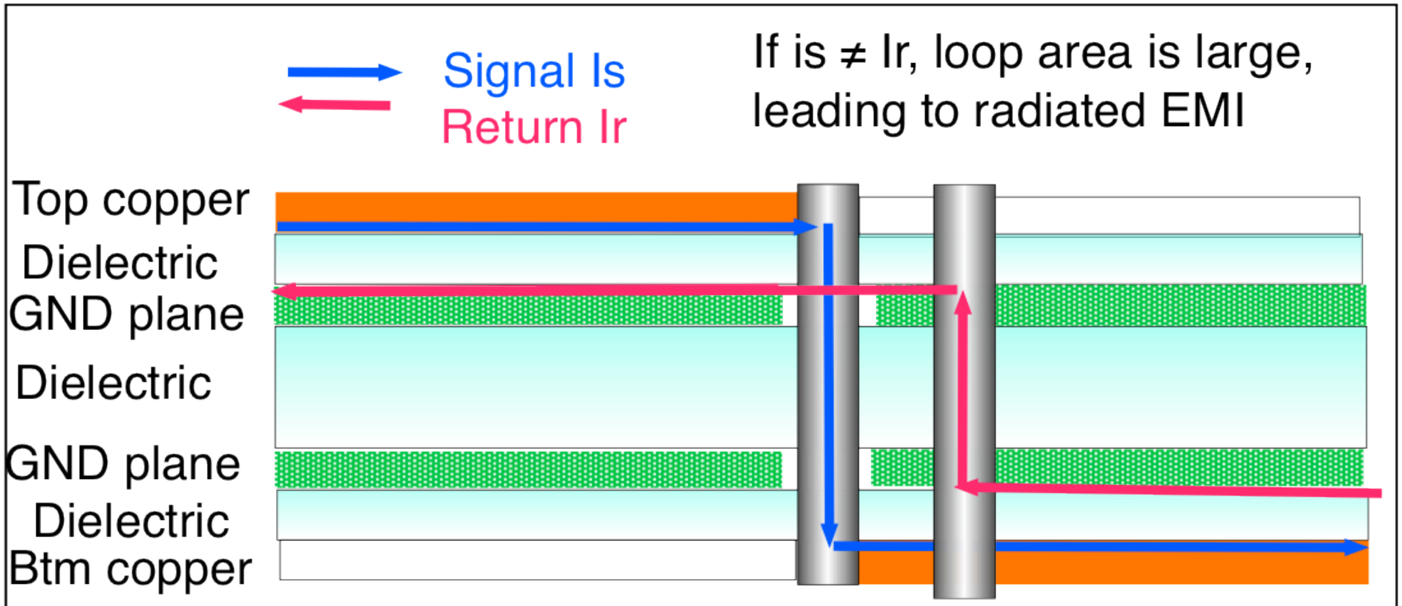
Changing Reference Planes



If is ≠ Ir, loop area is large, leading to radiated EMI

Case 2: Signal is via'd from one side of a reference plane to a separate reference plane. This is a problem as the **ground is not continuous**.

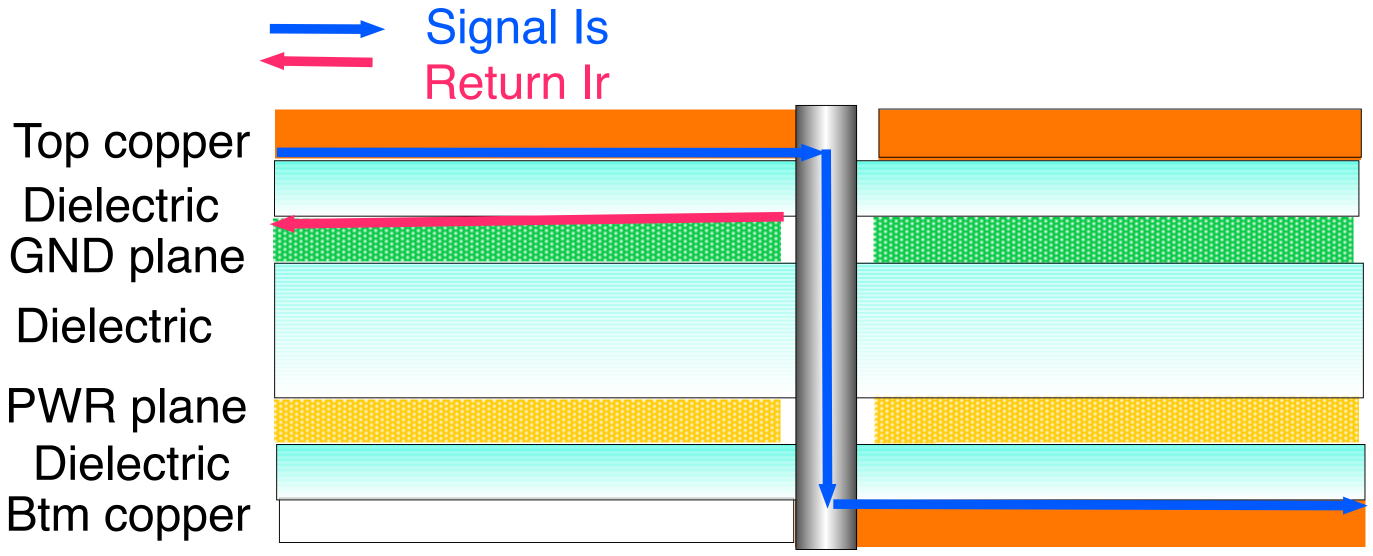
Changing Reference Planes



If is ≠ Ir, loop area is large, leading to radiated EMI

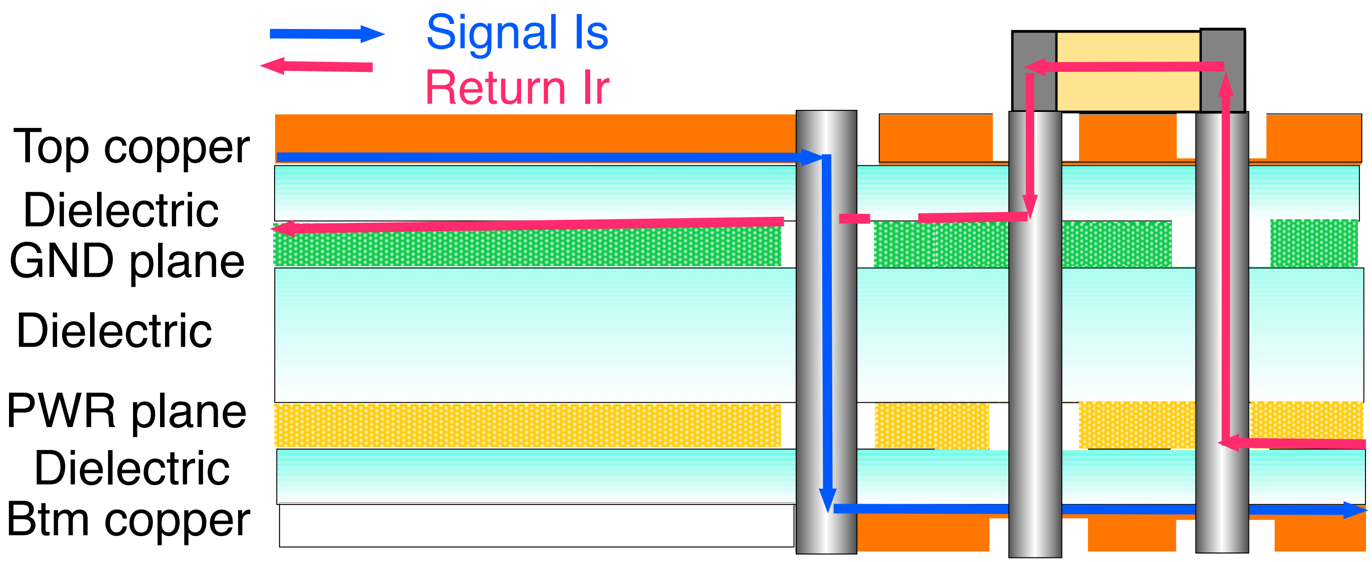
Case 2: Solution: Add GND via(s) between the reference planes adjacent to the signal via to provide a low RF impedance for the return. – **Even better – quad via surround of signal**

Isolated (e.g., power) Reference Planes



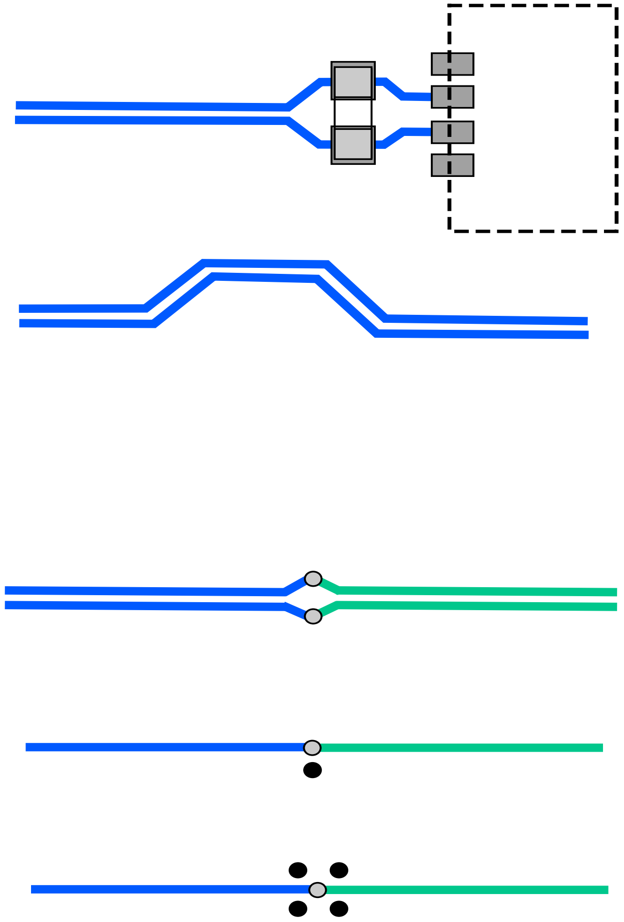
Case 3: Signal is via'd from a ground reference plane to an isolated (e.g., power) plane… No low impedance path for the RF return current.

Isolated (e.g., power) Reference Planes



Case 3: A small capacitor near the signal via with very low RF impedance to both planes (e.g., power and ground) provides a significantly improved return current path.

Some Tips

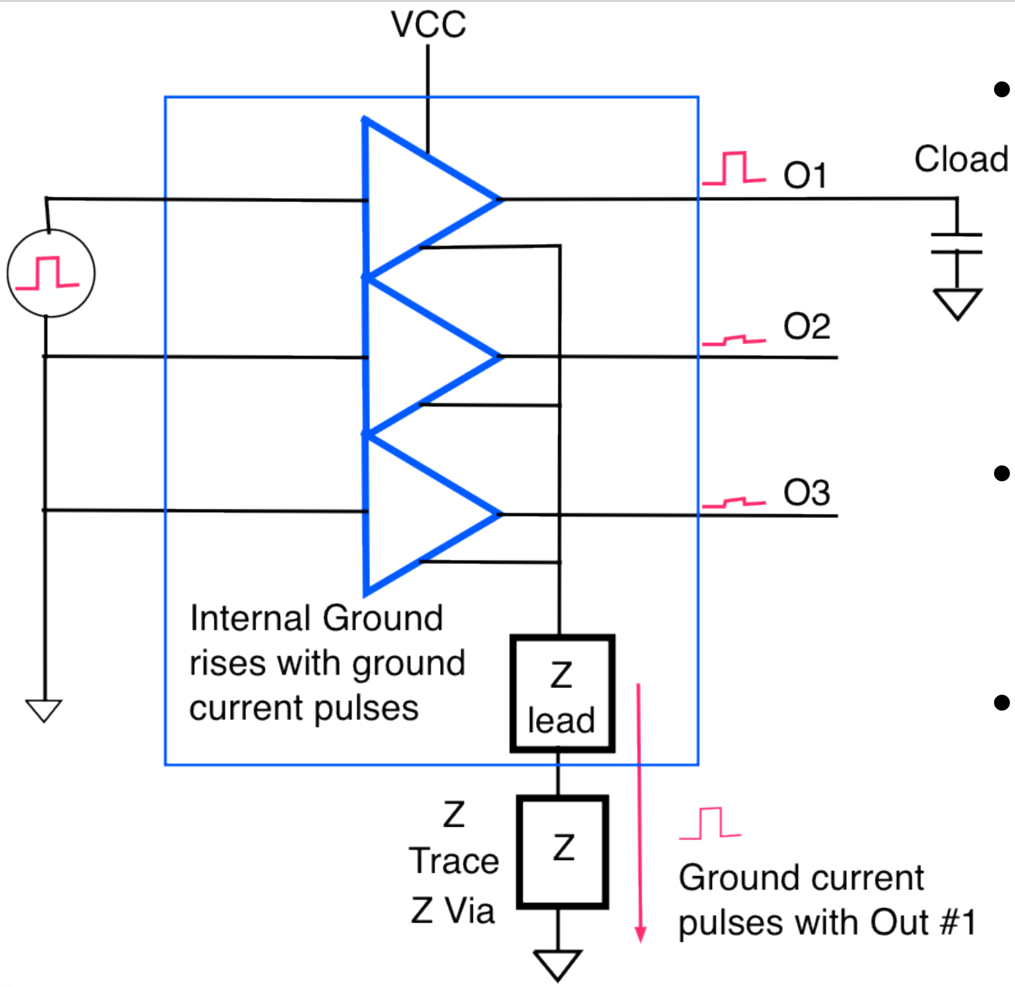


- Keep stubs after terminators very short
- Route through and terminate after pins for higher speed signals
- Route pairs in a balanced manor
- Use on-chip termination for very high speed signals
- If you must change layers, keep symmetry
- On Single Ended, place a GND via between the reference planes adjacent
- Even better: Use a Quad Via pattern

Summary: Avoiding the Discontinuous Ground Issues

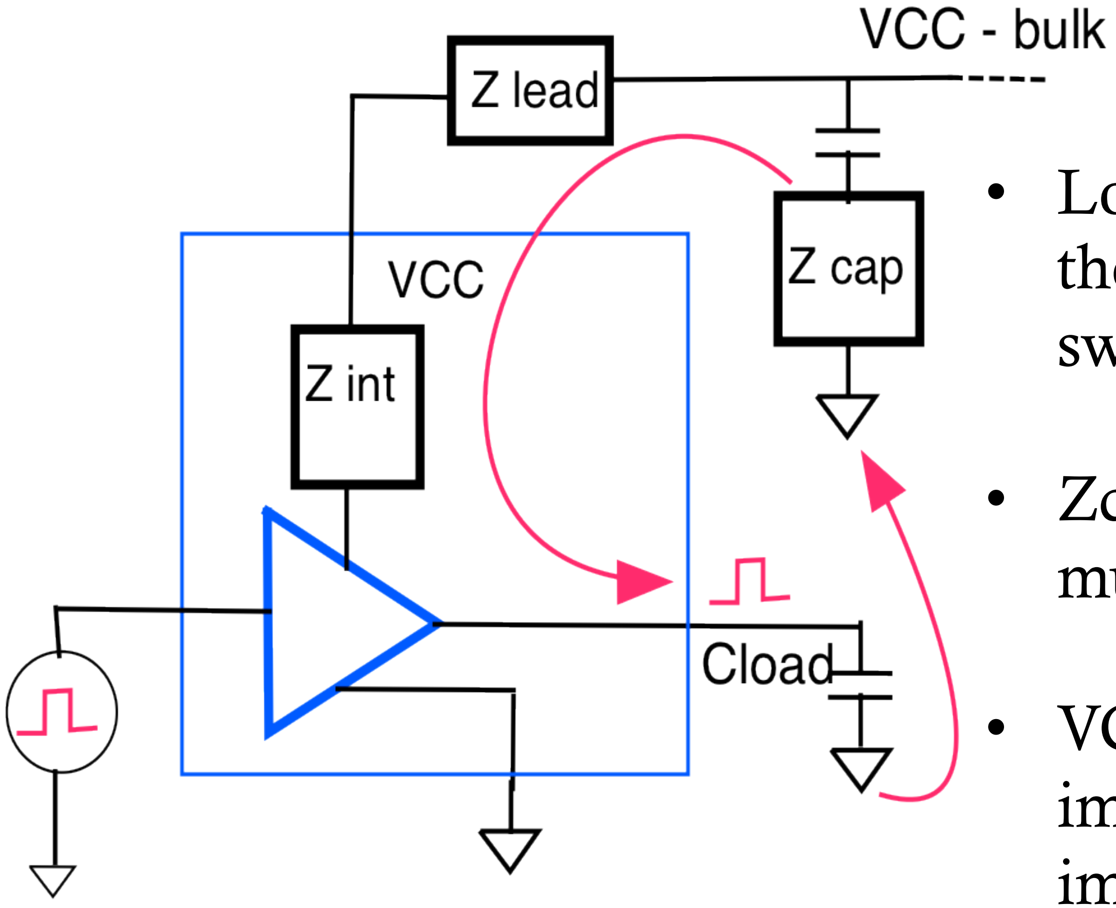
- **Use** Ground **Plane**(s). If possible, **avoid gaps in it**.
- **Don't route across gaps in planes** or change reference planes without ensuring a **low RF impedance path at or near the via**.
- Most important for **high rise-time, high duty cycle**, but **all** signals can cause EMI!
- Route **high speed traces** and **differential pairs** on a **single layer** if possible.

High Ground Impedance and Ground Bounce



- Switching currents are coupled to other outputs through common impedance
- Low speed signals still can contain RF
- Must keep ground impedance low!

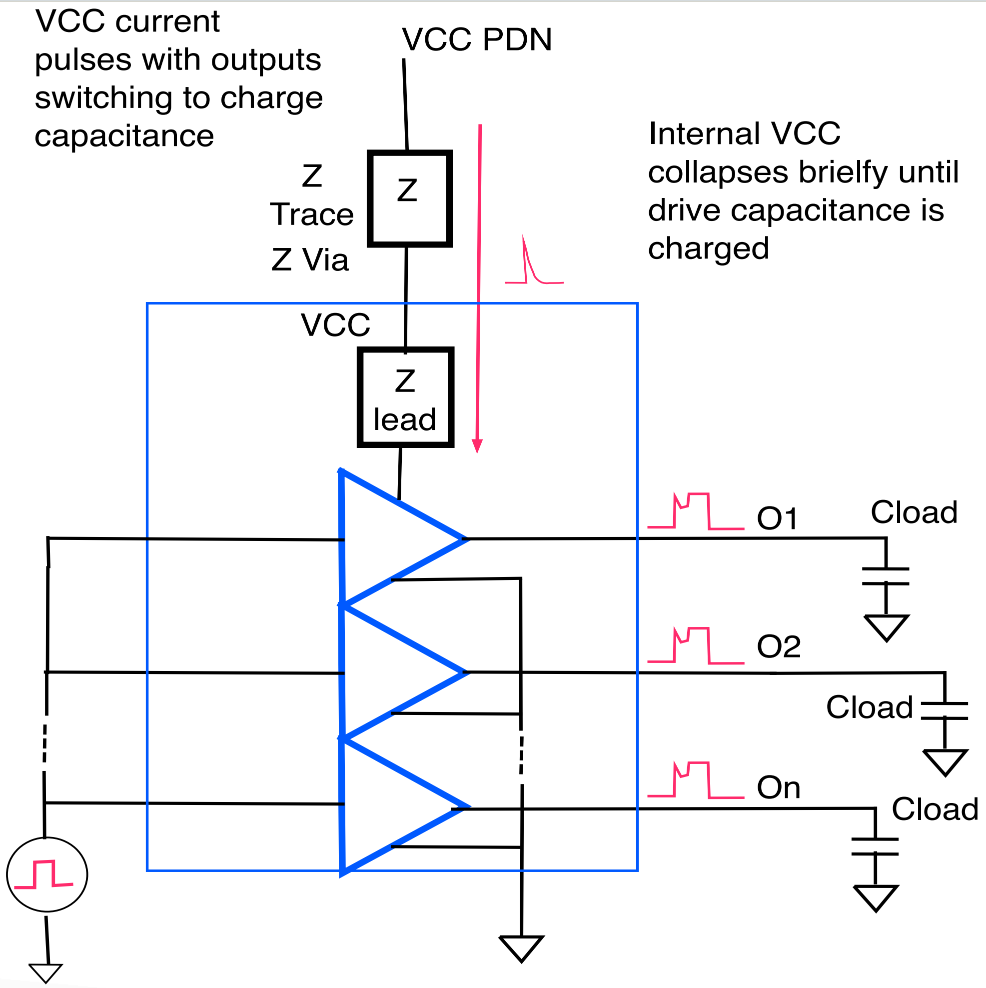
Good Bypass is Essential



Why Bypass?

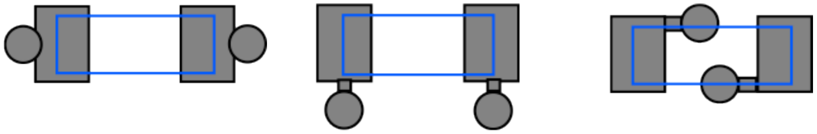
- Local HF caps provide the peak currents during switching
- Zcap, Zlead, and Zint must all be low at RF
- VCC bulk supply RF impedance is less important

4. High PDN Impedance and Power Bounce

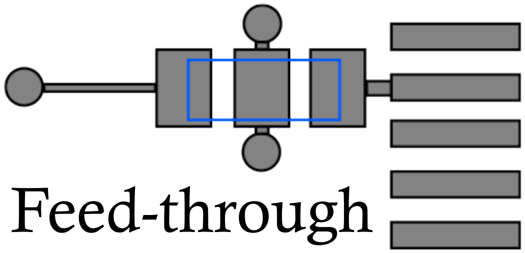


- Switching currents are coupled to outputs From VCC.
- Low speed signals still can contain RF
- Must keep PDN impedance low!
- Bypass Caps Essential

Bypass Layout for lower RF Impedance



Better →

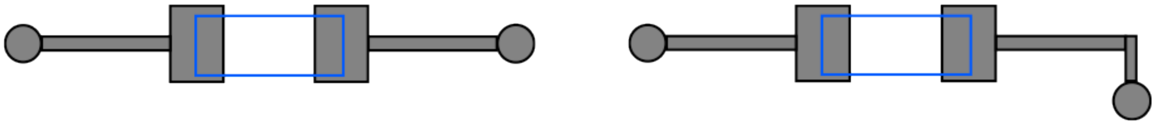


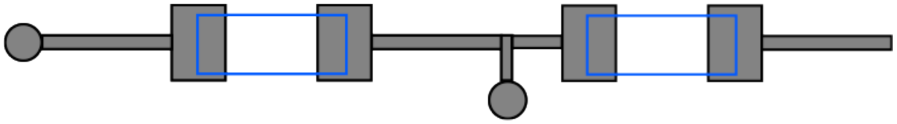
Feed-through Caps

Poor

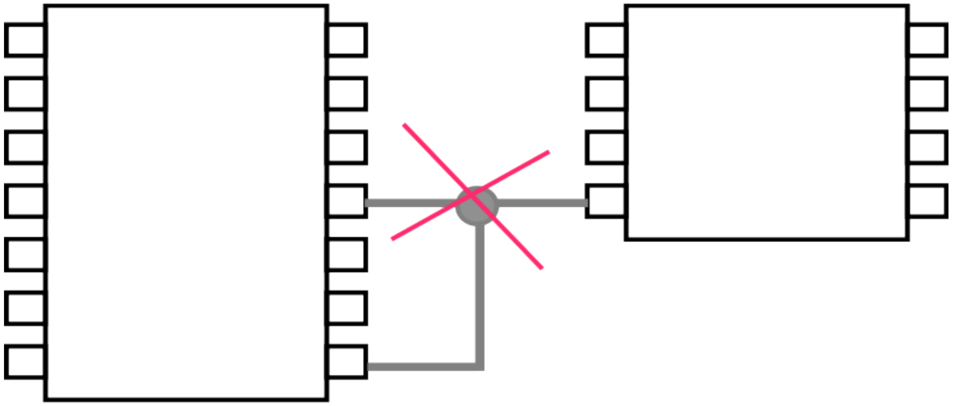
Note low-Z from power pin to cap and also from cap to GND

Terrible!

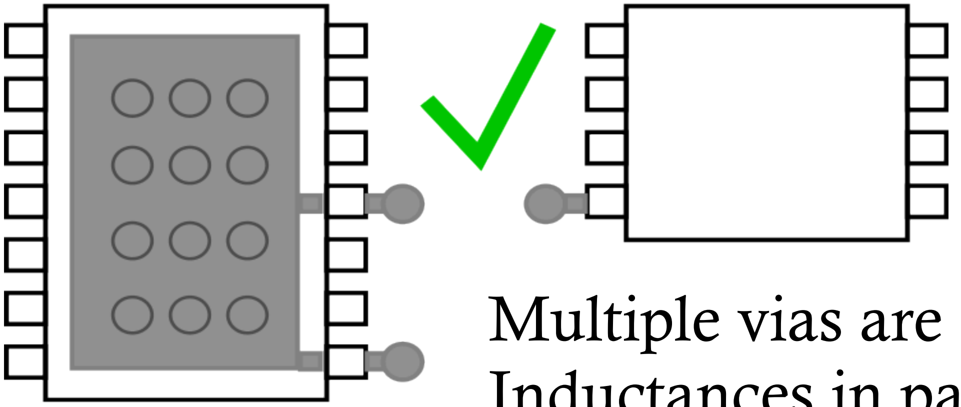




Avoid this common error!



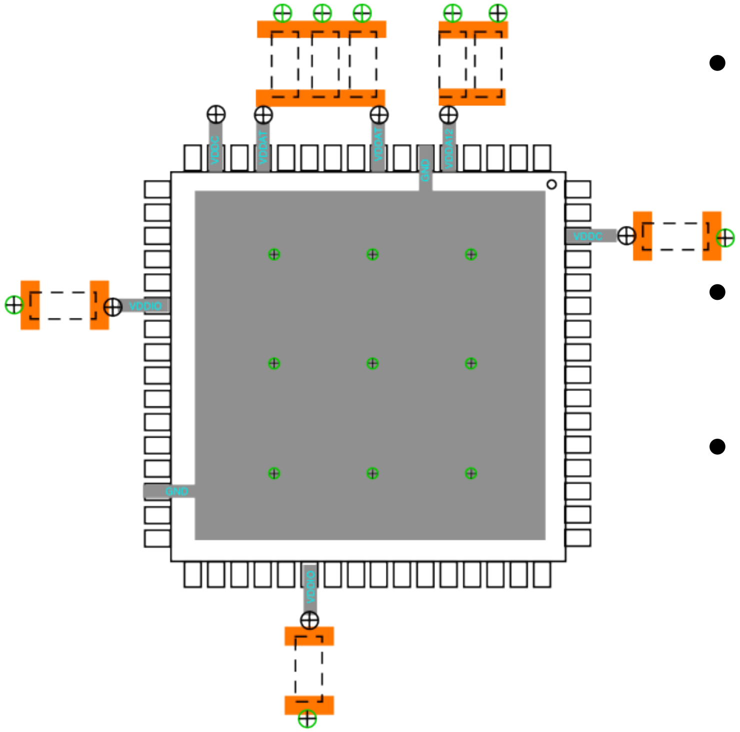
When layout personnel don’t understand ground bounce



Route Grounds carefully and watch out for auto-routers!

Multiple vias are even better …
Inductances in parallel divide.

Practical chip example – Bypass caps on opposite side

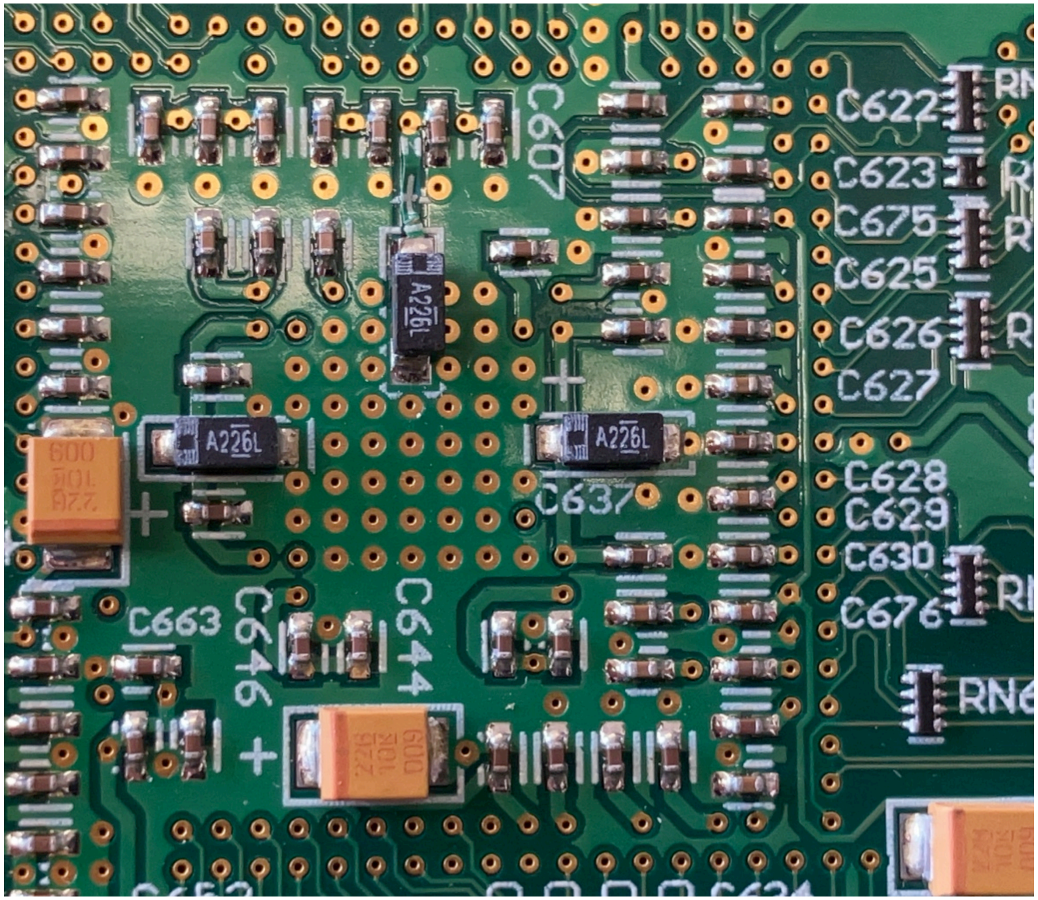


(Based on a Reference Design)

- Ground area under chip and return GND pins to this.
- Stitch all ground vias to the continuous ground plane.
- Make a supplemental ground plane where practical on the bottom layer.
- Power fed from internal planes.

Another Example BGA (caps un bottom side)

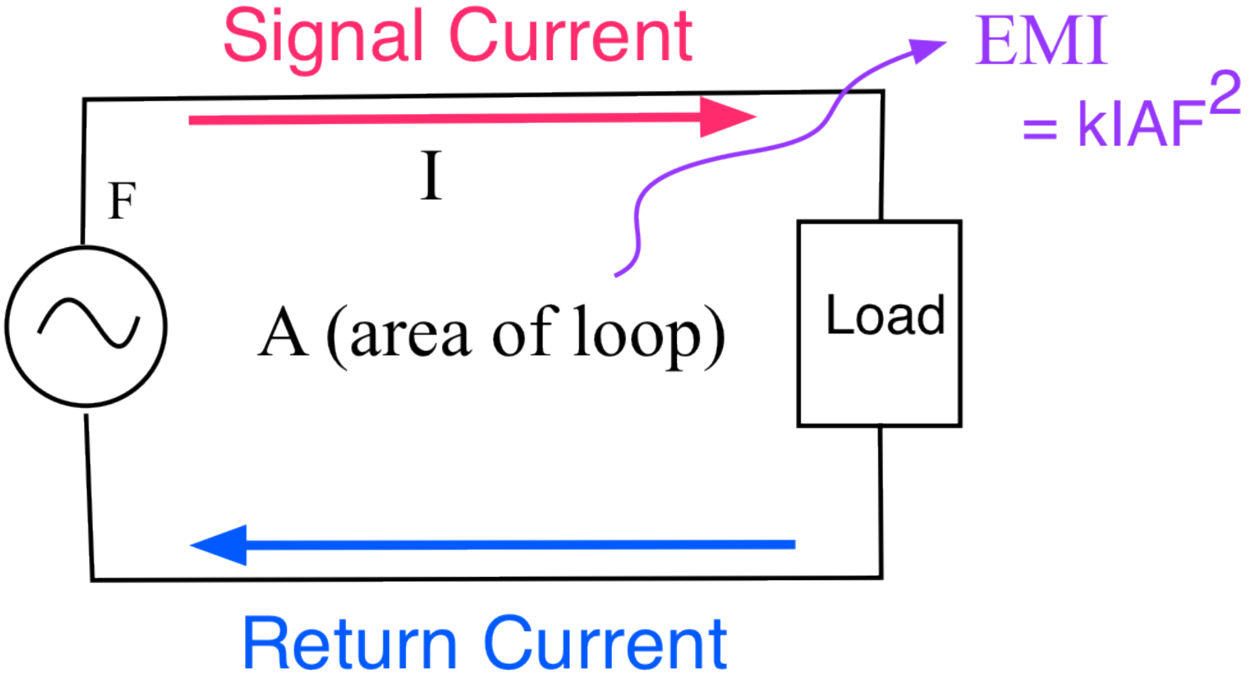
- Shortest practical route from BGA pads to Via to Caps.
- Cap immediately Returned to GND under BGA.
- GND Vias include inner GND plane and bottom side GND fill.
- Via in pad option was not available for this, but would reduce inductance.



Tips for Bypass, Ground and Power Bounce

- **Minimize Ground and Power Inductance**
  - **Never share ground vias or traces**. In fact **use multiple vias**. Via inductances in parallel reduce the total.
  - Keep ground traces **short and fat** (3:1)
  - Use a **continuous ground plane close to the routing layer** and use very **low impedance paths** for bypass caps
  - **TIP**: Use **series impedance on outputs** or IO to **reduce peak current spikes.**
  - Remember the ***ALL*** **outputs** can be **affected** by ground and power **bounce**… **not just the "fast"** signals.

EMI: Minimize the **loop area**

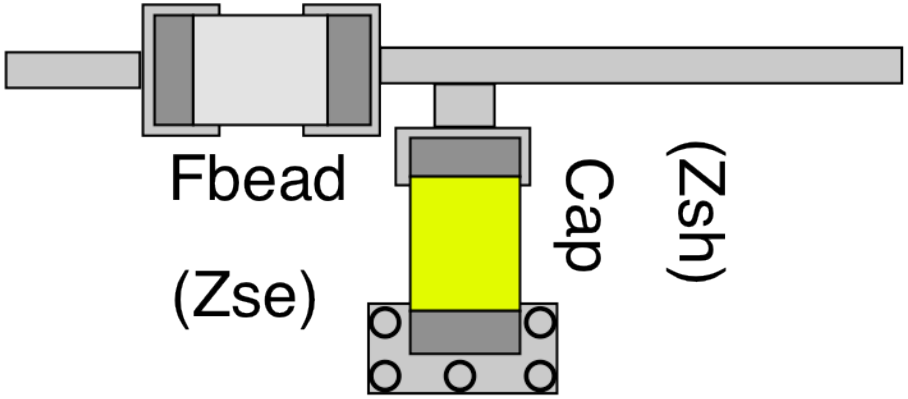


Pay attention to the return current path!

For **EMI – Shield** or **Filter** *All* IO

- **Every** signal **entering** or **exiting** must be **shielded** or **filtered** (or both)
- **Shielded** Cables – **must** connect connector shield to shield enclosure
- **Unshielded** cables (including shielded cables in a non-shielded enclosure) – **must** Filter!
- Need to **keep common mode noise off cables**
- Need to provide **low RF impedance signal return paths** – small loop areas

Example – add a series ferrite and a shunt capacitor



Typical Ferrite:
100 ohms at 100 MHz

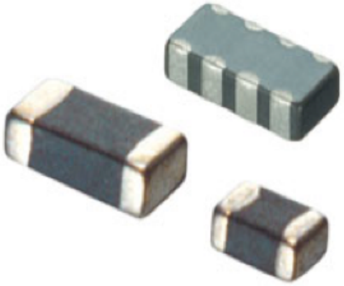
Cap 0.001 uF:
1.6 ohms at 100 MHz

Attenuation ≈
1.6/100 - about 36 dB

(neglecting trace impedance and esr)

Some options for RF filtering IO

- Series Impedance
  - Ferrite or Resistor

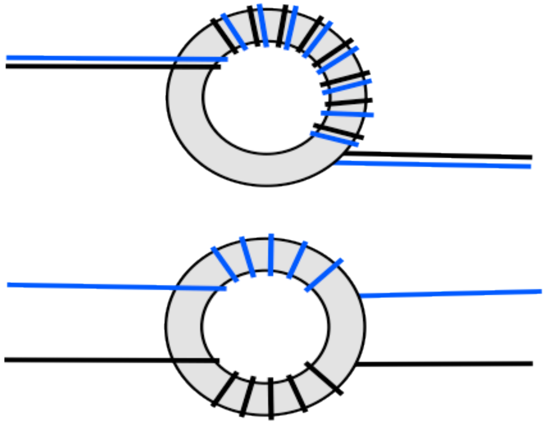


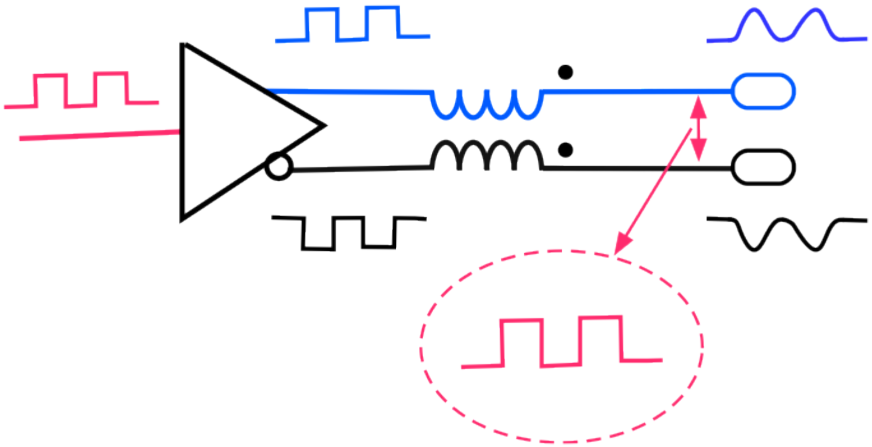
- Shunt Cap to Ground reference

- Tee or Pi 3-terminal Filter, F-T Cap

- Common Mode Choke

Common Mode Chokes





- Two windings share magnetic field
- Fields cancel for Normal Mode – Low Z
- Fields add for Common Mode – High Z

- Differential (Normal) signal OK
- Common mode is blocked
- No Ground Needed

Summing up…

- Remember the "**Hidden Schematic**"
- Start with a **good PCB Stack up** plan -- Pay particular attention to a **solid ground (reference plane)** structure
- **Avoid Impedance** and **Return Path Discontinuities**
- Pay close attention to **return currents** and **return current paths**. **Don't unbalance** balanced lines.

Summing up…

- **Identify high speed lines** and give them **priority**.
  - High**est speed** on **single layer**
  - Keep **Differential lines** together and **balanced**.
- Take **great care in bypassing** to keep **series impedance at RF** ***very*** **low**.
- Group (if possible) and **Filter all IO**

Questions?

Thank You!

Stop by the ESDI
table for more Info

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